

CAS CS 561: Data Systems Architectures Data-intensive Systems and Computing Lab Department of Computer Science College of Arts and Sciences, Boston University <u>http://bu-disc.github.io/CS561/</u>



CS561 Spring 2025 - Research Project

Title: *Performance study of Bufferpool Manager on Emulated SSDs*

Background: Storage devices like Solid State Drives (SSDs) can achieve high bandwidths because of the internal architecture and block mapping mechanisms. However, the applications still need to optimize their algorithms to take advantage of the device's internal parallelism. Recent research has developed systems like ACE, Asymmetry & Concurrency-aware bufferpool manager. ACE batches writes and issues them in parallel to exploit SSD's concurrency. For this study we propose using a block interface SSD emulator FEMU. This emulator allows fine-grained control over SSD configuration such as number of chips, channels, block mapping and striping mechanisms.

Objective: The objective of the project is to analyze ACE's performance across various SSD configurations. The project may also involve adding some functionality to the emulator's FTL.

Steps:

- Explore the SSD architecture and configuration options through the emulator
- Understand the ACE's design, and how to run PostgreSQL in the virtual machine for the SSD emulator
- As an initial experiment use FEMU to emulate block interface SSDs with different number of channels, ways and mapping mechanisms currently supported by the emulator. Experiment with ACE's performance across various SSD configurations.

Responsible mentor: Teona Bagashvili

References

[1]Papon, Tarikul Islam, and Manos Athanassoulis. "ACEing the Bufferpool Management Paradigm for Modern Storage Devices." 2023 IEEE 39th International Conference on Data Engineering (ICDE). IEEE, 2023.

[2]Li, Huaicheng, et al. "The {CASE} of {FEMU}: Cheap, accurate, scalable and extensible flash emulator." 16th USENIX Conference on File and Storage Technologies (FAST 18). 2018.