# Persistent B+-Tree in Non-Volatile Main Memory

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#### Non Volatile Memory

#### Data Structure









Non Volatile Memory

- do not need power to retain data
- enable smaller feature size

#### Туре

- Phase Change Memory (PCM)
- Ferroelectric RAM (F-RAM)
- Magnetoresistive RAM (MRAM)



#### Growth in main memory



B+ Tree







Inconsistent





x86 instructions

- clflush
- mfence





x86 instructions

- clflush
- mfence



#### Challenge





- Follows 2 traditional Principles:
   Logging
  - Shadowing



- Records REDO and UNDO information, for every update, in a log
- Log: an ordered list of REDO/UNDO actions
  - Contains information of each update
- Ensures the database fulfills the **atomicity** principle



### Shadowing

- The process of creating multiple copies of data.
- Ensures that the original data is not being updated till the very end to ensure database is **durable**



Shadow-copy technique for atomicity and durability

## **Undo-Redo Logging**

Divide memory into 2 parts:

- **Persistent**: Holds persistent tree nodes
- Volatile: stores the buffer pool

To protect in-place NVM writes requires undo-redo logging

• Requires **clflush** and **mfence** to ensure log content is stable before performing actual write

2:	log.write (addr, *addr, newValue);
3:	log.clflush_mfence ();
4:	*addr= newValue;
5:	end procedure
6:	procedure NEWREDO(addr,newValue)
7:	log.write (addr, newValue);
8:	*addr= newValue;
9:	end procedure
0:	procedure COMMITNEWREDO
1:	log.clflush_mfence ();
2:	end procedure

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4:	*addr= newValue;
5:	end procedure
6:	procedure NEWREDO(addr,newValue)
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Figure 5: NVMM write protected by undo-redo logging.

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	11:	log.clflush_mfence ();
<b>)</b>	12:	end procedure
-		

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Figure 5: NVMM write protected by undo-redo logging.

## **Logging Continued**

- Only applicable if a newly written value is not to be accessed again before commit
- Re-reading the **newly written** value **before commit** will cause an **error**.

1: 2: 3:	<pre>procedure WRITEREDOONLY(addr,newValue)     log.write (addr, newValue); end procedure</pre>
4:	procedure COMMITREDOWRITES
5:	log.clflush_mfence ();
6:	for all (addr,newValue) in log do
7:	*addr= newValue;
8:	end for
9:	end procedure

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9:	end procedure

Figure 6: Redo-only logging.

## Shadowing

#### • Short-Circuit Shadowing

- Taking advantage of the 8 byte atomic write feature in NVM.
- Automatically modify the leaf node pointer in the updated node's parent.
- A single 8 byte pointer points to newly created node copy

2:	copyLeaf= AllocNode();
3:	NodeCopy(copyLeaf, leaf);
4:	Insert(copyLeaf, newEntry);
5:	<pre>for i=0; i &lt; copyLeaf.UsedSize(); i+=64 do</pre>
6:	clflush(&copyleaf + i);
7:	end for
8:	WriteRedoOnly(&parent.ch[ppos], copyLeaf);
9:	WriteRedoOnly(&sibling.next, copyLeaf);
10:	CommitRedoWrites();
11:	FreeNode(leaf);
12: e	nd procedure

Figure 7: Shadowing for insertion when there is no node splits.

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3:	NodeCopy(copyLeaf, leaf);
4:	Insert(copyLeaf, newEntry);
<b>D</b> :	for 1=0; 1 < copyLeaf.UsedSize(); 1+=64 do
6:	clflush(&copyleaf + i);
7:	end for
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Figure 7: Shadowing for insertion when there is no node splits.

#### Write Atomic B+-Trees

#### **Design Goals:**

- Atomic write to commit all changes
- Minimize the movement of index entries
- Good search performance

#### wB+ - Tree Structures

- Introduced a small indirection array to a bitmap-only unsorted node.
- Slot+Bitmap nodes contain both a bitmap and indirection slot array.
- Combine slot-only nodes, slot+bitmap nodes, bitmap-only leaf nodes to form 3 wB+ - Tree structures

Slot array 5	$bmp k_1 k_2 \circ \circ \circ k_n$
Index entries 9 2 3 1 7	next $p_1 p_2 \circ \circ \circ p_n$
(a) Slot array with 1-byte slots	(b) Bitmap-only leaf
slot $k_1 = k_2 \circ \circ \circ k_n$	slot $k_1 k_2 \circ \circ \circ k_n$
$ch_0 ch_1 ch_2 \circ \circ \circ ch_n$	next $p_1 p_2 \circ \circ \circ p_n$
(c) Slot-only nonleaf (n<8)	(d) Slot-only leaf (n<8)
slot bmp k <sub>1</sub> ooo k <sub>n'</sub>	slotbmp_k1_000_k_n'
array $herefore h_0 ch_1 \circ \circ \circ ch_{n'}$	array next p <sub>1</sub> ooo p <sub>n</sub>
(e) Slot+bitmap nonleaf	(f) Slot+bitmap leaf

Figure 8:  $wB^+$ -Tree node structures. (For a slot+bitmap node, the lowest bit in the bitmap indicates whether the slot array is valid. Slot 0 records the number of valid entries in a node.)

Table 2:	wB <sup>+</sup> -Tre	e structures	considered	in	this	paper.
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Structure	Leaf Node	Non-leaf Node
wB <sup>+</sup> -Tree	slot+bitmap leaf	slot+bitmap non-leaf
wB <sup>+</sup> -Tree w/ bitmap-only leaf	bitmap-only leaf	slot+bitmap non-leaf
wB <sup>+</sup> -Tree w/ slot-only nodes	slot-only leaf	slot-only non-leaf

## **Insertion (Slot only)**



Insert position in slot array: 1 Unused entry offset: 3

1:	procedure INSERT2SLOTONLY_ATOMIC(leaf, newEntry)
2:	/* Slot array is valid */
3:	<pre>pos= leaf.GetInsertPosWithBinarySearch(newEntry);</pre>
4:	/* Write and flush newEntry */
5:	u= leaf.GetUnusedEntryWithSlotArray();
6:	leaf.entry[u]= newEntry;
7:	clflush(&leaf.entry[u]); mfence();
8:	/* Generate an up-to-date slot array on the stack */
9:	for $(j=leaf.slot[0]; j \ge pos; j)$ do
10:	tempslot[j+1]= leaf.slot[j];
11:	end for
12:	tempslot[pos]=u;
13:	for (j=pos-1; j>1; j) do
14:	tempslot[j]= leaf.slot[j];
15:	end for
16:	tempslot[0]=leaf.slot[0]+1;
17:	/* Atomic write to update the slot array */
18:	*((UInt64 *)leaf.slot)= *((UInt64 *)tempslot);
19:	clflush(leaf.slot); mfence();
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1: procedure INSERT2SLOTBMP\_ATOMIC(leaf, newEntry) 2: if (leaf.bitmap & 1 == 0) /\* Slot array is invalid? \*/ then Recover by using the bitmap to find the valid entries, 3: building the slot array, and setting the slot valid bit; 4: end if 5: pos= leaf.GetInsertPosWithBinarySearch(newEntry); 6: /\* Disable the slot array \*/ 7: leaf.bitmap = leaf.bitmap - 1; 8: clflush(&leaf.bitmap); mfence(); 9: /\* Write and flush newEntry \*/ 10: u= leaf.GetUnusedEntryWithBitmap(); 11: leaf.entry[u]= newEntry; 12: clflush(&leaf.entry[u]); 13: /\* Modify and flush the slot array \*/ 14: for (j=leaf.slot[0]; j>pos; j - -) do 15: leaf.slot[j+1]= leaf.slot[j]; 16: end for 17: leaf.slot[pos]=u; 18: for (j=pos-1; j>1; j - -) do 19: leaf.slot[j]= leaf.slot[j]; 20: end for 21: leaf.slot[0]=leaf.slot[0]+1; 22: for  $(j=0; j \le leaf.slot[0]; j += 8)$  do 23: clflush(&leaf.slot[j]); 24: end for 25: mfence(); /\* Ensure new entry and slot array are stable \*/ 26: /\* Enable slot array, new entry and flush bitmap \*/ 27: leaf.bitmap = leaf.bitmap + 1 + (1 << u); 28: clflush(&leaf.bitmap); mfence(); 29: end procedure



Insert position in slot array: 1 Unused entry offset: 3

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4:	end if
5:	pos= leaf.GetInsertPosWithBinarySearch(newEntry);
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7:	leaf.bitmap = leaf.bitmap - 1;
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19:	<pre>leaf.slot[j]= leaf.slot[j];</pre>
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26:	/* Enable slot array, new entry and flush bitmap */
27:	leaf.bitmap = leaf.bitmap + 1 + (1 << u);
-	10 1/01 01: 5 0 0

#### **Insertion - Node Split**

Insert 9





### **Deletion**

#### **Deletion:**

- Does not move data around
- Modify slot array and/or bitmap to reflect deletion



#### Search

#### Search:

- Apply binary search on slot array
- Stop binary search when range < 8 slots for lower overhead



## Variable Sized Key

Solution:

• Store 8-byte pointers to key

Disadvantage:

- Key pointer dereference overhead
- Larger keys takes longer to retrieve & process



### **Comparison With Previous Solutions**

Term	Description
$N_w$	Number of words written to NVMM
Nclf	Number of cache line flush operations
$N_{mf}$	Number of memory fence operations
n	Total number of entries in a B <sup>+</sup> -Tree node
n'	Total number of entries in a wB <sup>+</sup> -Tree node
m	Number of valid entries in a tree node
l	Number of levels of nodes that are split in an insertion

B <sup>+</sup> -Trees undo-redo logging	$N_w = 4m + 12,$ $N_{clf} = N_{mf} = m + 3$
B <sup>+</sup> -Trees shadowing	$  N_w = 2m + 11, N_{mf} = 2, \\ N_{clf} = 0.25m + 2.5 $
wB <sup>+</sup> -Tree	$N_w = 0.125m + 4.25, N_{clf} = \frac{1}{64}m + 3\frac{1}{32}, N_{mf} = 3$

### **Evaluation**

**Experiment Setup** 

- B+ trees implementations:
   9 different trees
- 2. Memcached Implementation
- 3. B+ tree workload

#### Table 4: Experimental Setup.

	Real Machine Description
Processor	2 Intel Xeon E5-2620, 6 cores/12 threads, 2.00GHz
CPU cache	32KB L1I/core, 32KB L1D/core, 256KB L2/core 15MB shared L3, all caches with 64B lines
OS Compiler	Ubuntu 12.04, Linux 3.5.0-37-generic kernel gcc 4.6.3, compiled with -O3
	Simulator Description
Processor	Out-of-order X86-64 core, 3GHz
CPU cache	Private L1D (32KB, 8-way, 4-cycle latency), private L2 (256KB, 8-way, 11-cycle latency), shared L3 (8MB, 16-way, 39-cycle latency), all caches with 64B lines, 64-entry DTLB, 32-entry write back queue
РСМ	4 ranks, read latency for a cache line: 230 cycles, write latency per 8B modified word: 450 cycles, $E_{rb} = 2$ pJ, $E_{wb} = 16$ pJ

Computer for experiment

#### **Simulation Modeling PCM**



#### **Simulation Modeling PCM**



#### **Real Machine Experiments Modeling Fast DRAM-Like NVM**



#### **Real Machine Experiments for Trees with String Keys**



#### **Real-Machine Memcached Performance**





**Logging** and **shadowing** incurs high overhead due to **NVM writes** & **CL flushes**.

The factors affecting performance have **different weights** for **different NVM technologies**.

wB+-Trees **significantly improve** the **insertion** and **deletion** performance while achieving good **search** performance.

#### Thank you!

